电 话：0755-27668030 27668083　　传 真：0755-27668030-606

Specifications for Approval

Customer: _____

Model name: YJD1602A-1　VER:　V 1.0

ISSUE	QC DEPT	APPROVAL

Customer Approval
☐ Accept　☐ Reject Comment: Approval by:

确认后请将此页回传

DATE: 2007-09-08

YJD1602A-1 LCD MODULE
(CHARACTER Type)

1.0 FEATURES

- **Display Mode: STN, Positive（Negatative）, Transmissive Yellow-Green（Blue）**
- **Display Formate: 16 Character x 2 Line**
- **Viewing Direction: 6：00'Clock**
- **Input Data: 4-Bits or 8-Bits interface avaliable**
- **Display Font : 5 x 8 Dots**
- **Power Supply : Single Power Supply (5V±10%)**
- **Driving Scheme : 1/16Duty,1/5Bias**
- **Control IC: S6A0069 S6A0065**
- **Backlight (Side)：LED Yellow-Green （chalkiness）**

2.0 ABSOLUTE MAXIMUM

Item	Symbol	Min.	Max.	Unit
Power Supply for logic	Vdd	-0.3	+6.0	V
Power supply for LCD Drive	Vlcd	Vdd-11.5	Vdd+0.3	V
Input Voltage	Vi	-0.3	Vdd+0.3	V
Operating Temperature	Ta	0	+50	℃
Storage Temperature	Tstg	-10	+60	℃

3.0 ELECTRICAL CHARACTERISTICS

(Ta=25℃;Vdd=3.0V±10%,otherwise specified)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power Supply for Logic	Vdd	--	4.7	5.0	5.5	V
Operating Voltage for LCD	Vdd-Vo	--	--	5.0	--	V
Input High voltage	Vih	--	2.2	--	Vdd	V
Input Low voltage	Vil	--	-0.3	--	0.6	V
Output High voltage	Voh	-Ioh=0.2mA	2.4	--	--	V
Output Low voltage	Vol	Iol=1.2mA	--	--	0.4	V
Power supply current	Idd	Vdd=3.0v	--	--	--	mA

4.0 MECHANICAL PARAMETERS

Item	Description	Unit
PCB Dimension	80.0*36.0*1.6	mm
View Dimension	64.0*13.5	mm
Outline Dimension	80.0*36.0*14.0	mm

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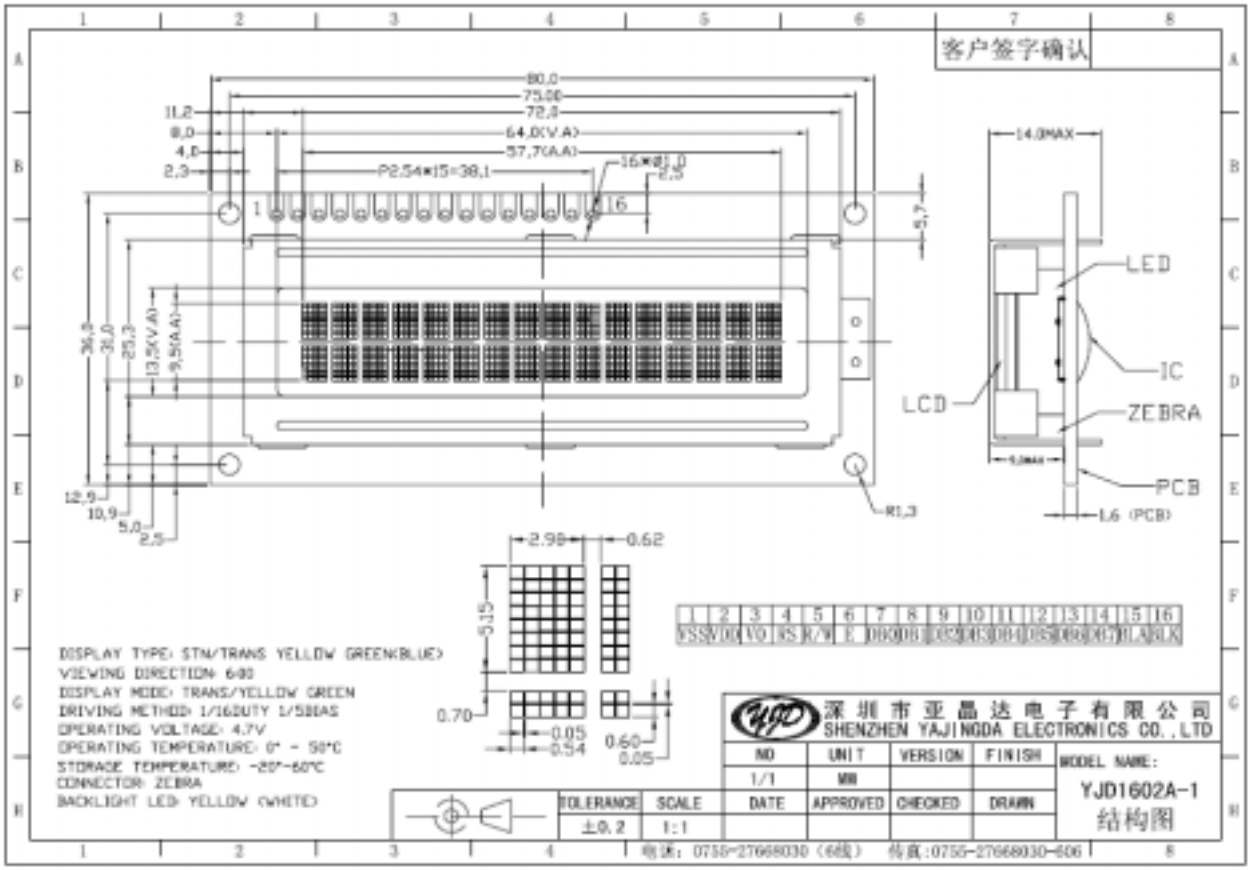
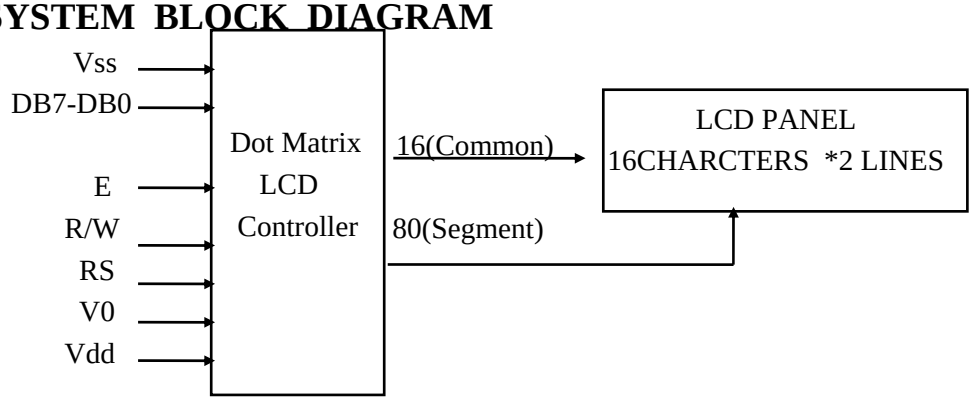
5.0 PIN ASSIGNMENT

No.	Symbol	Level	Function	
1	VSS	--	+0V	Power Supply
2	VDD	--	+5V	
3	V0	--	for LCD	
4	RS	H/L	Register Select: H:Data Input L:Instruction Input	
5	R/W	H/L	H--Read L--Write	
6	E	H,H-L	Enable Signal	
7--10	DB0-- DB3	H/L	Data bus used in 8 bit transfer	
11--14	DB4-- DB7	H/L	Data bus for both 4 and 8 bit transfer	
15	BLA	----	Power for LED Backlight (+5 V)	
16	BLK	----	Power for LED Backlight (Ground)	

6.0 EXTERNAL DIMENSIONS



7.0 SYSTEM BLOCK DIAGRAM



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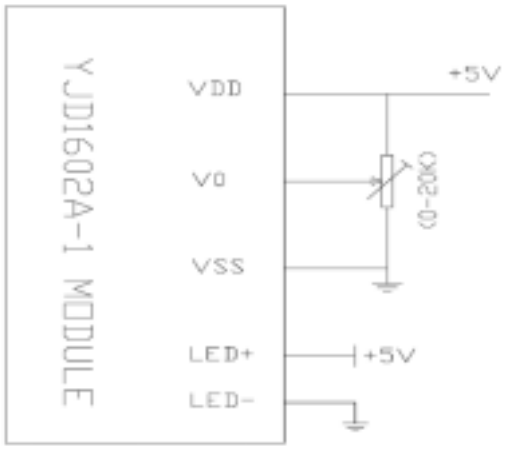
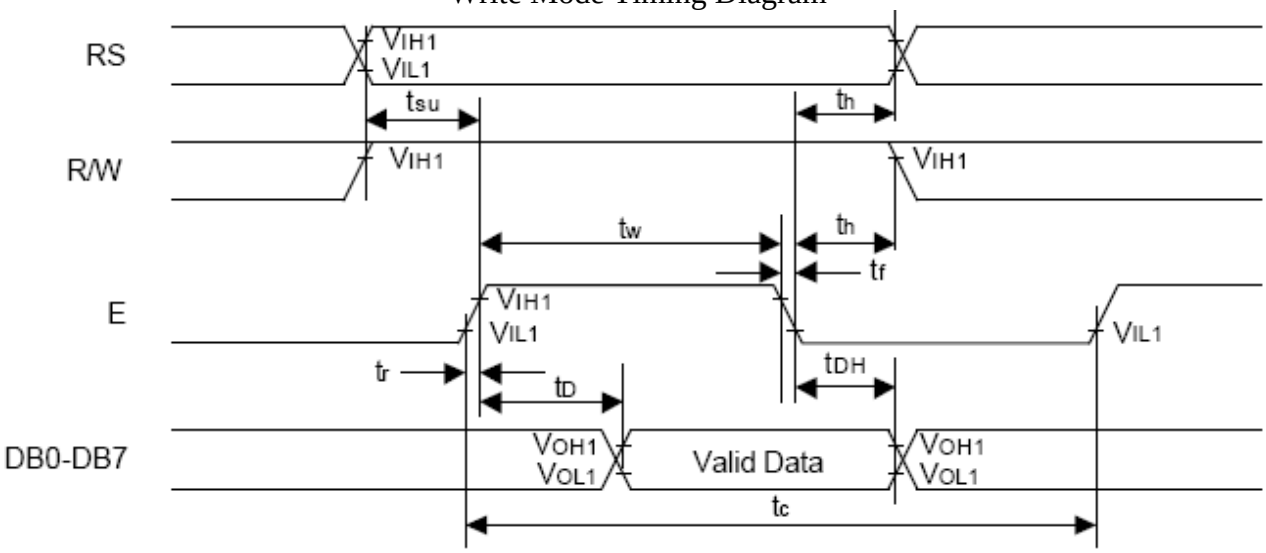
8.0 POWER SUPPLY BLOCK DIAGRAM

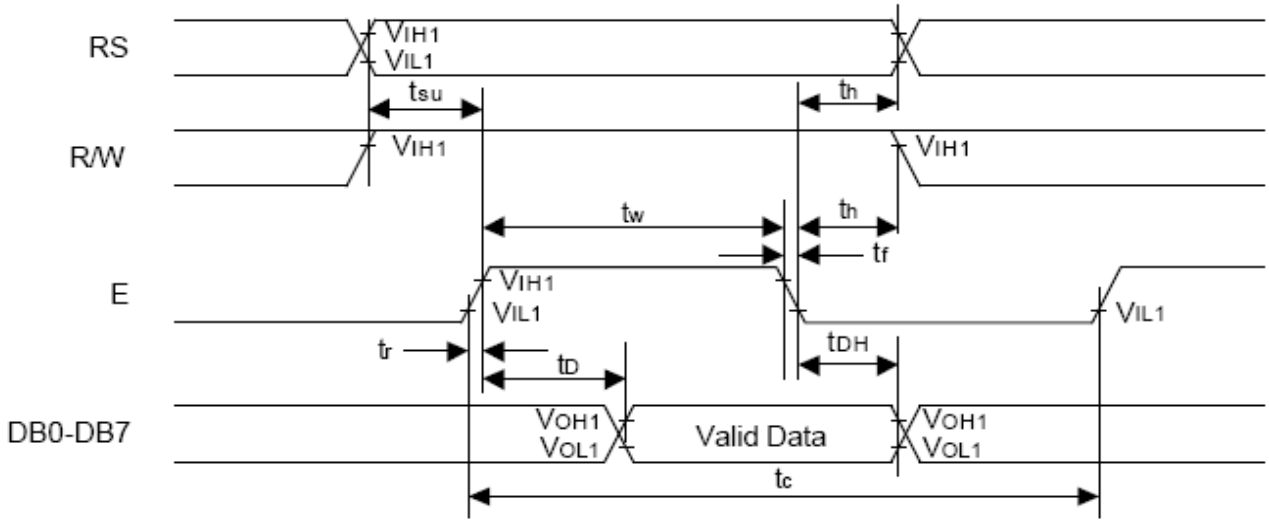


9.0 TIMING CHARACTERISTICS

Write Mode Timing Diagram



Read Mode Timing Diagram



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10.0 Display control instruction

The display control instructions control the internal state of the S6A0069. Instruction is received from MPU to S6A0069 for the display control. The following table shows various instructions.

Instruction	Instruction Code										Description	Execution
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Instruction Code	time(fsoc=270)
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM. and set DDRAM address to "00H" from AC.	1.53ms
Return Home	0	0	0	0	0	0	0	0	1	X	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.53ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction and make shift of entire display enable.	39μs
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Set display(D), cursor(C), and blinking of cursor(B) on/off control bit.	39μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	X	X	Set cursor moving and display shift control bit, and the direction, without changing DDRAM data.	39μs
Function Set	0	0	0	0	1	DL	N	F	X	X	Set interface data length (DL : 4-bit/8-bit), numbers of display line (N : 1-line/2-line), display font type (F : 5 X 8 dots/ 5 X 11 dots)	39μs
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	39μs
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.	39μs
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0μs
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	43μs
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	43μs

NOTE: When an MPU program with checking the Busy Flag (DB7) is made, it must be necessary 1/2 fosc is necessary for executing the next instruction by the falling edge of the "E" signal after the Busy Flag (DB7) goes to "LOW".

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INSTRUCTION DESCRIPTION

OUTLINE

To overcome the speed difference between internal clock of S6A0069 and MPU clock, S6A0069 performs internal operation by storing control information to IR or DR. The internal operation is determined according to the signal from MPU, composed of read/write and data bus. Instruction can be divided largely four kinds,

(1) S6A0069 function set instructions (set display methods, set data length, etc.)

(2) Address set instructions to internal RAM

(3) Data transfer instructions with internal RAM

(4) Others

The address of internal RAM is automatically increased or decreased by 1.

NOTE

During internal operation, Busy Flag (DB7) is read High. Busy Flag check must precede the next instruction. When an MPU program with checking the Busy Flag (DB7) is made, it must be necessary 1/2 fosc for executing the next instruction by the falling edge of the 'E' signal after the Busy Flag (DB7) goes to "LOW".

CONTENTS

Clear Display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status, namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = "1").

Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	–

Return Home is cursor return home instruction. Set DDRAM address to "00H" into the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM does not change.

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Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	SH

Set the moving direction of cursor and display.

I/D : Increment/decrement of DDRAM address (cursor or blink)
When I/D = "High", cursor/blink moves to right and DDRAM address is increased by 1.
When I/D = "Low", cursor/blink moves to left and DDRAM address is decreased by 1.
* CGRAM operates the same as DDRAM, when read from or write to CGRAM.

SH: Shift of entire display

When DDRAM read (CGRAM read/write) operation or SH = "Low", shift of entire display is not performed. If SH = "High" and DDRAM write operation, shift of entire display is performed according to I/D value (I/D = "1" : shift left, I/D = "0" : shift right).

Display ON/OFF Control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.

D : Display ON/OFF Control Bit
When D = "High", entire display is turned on.
When D = "Low", display is turned off, but display data is remained in DDRAM.

C : Cursor ON/OFF Control Bit
When C = "High", cursor is turned on.
When C = "Low", cursor is disappeared in current display, but I/D register remains its data.

B : Cursor Blink ON/OFF Control Bit
When B = "High", cursor blink is on, that performs alternate between all the high data and display character at the cursor position.
When B = "Low", blink is off.

Cursor or Display Shift

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	–	–

Shifting of right/left cursor position or display without writing or reading of display data. This instruction is used to correct or search display data (Refer to table 5). During 2-line mode display, cursor moves to the 2nd line after the 40th digit of the 1st line. Note that display shift is performed simultaneously in all the lines. When displayed data is shifted repeatedly, each line is shifted individually. When display shift is performed, the contents of the address counter are not changed.

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Shift Patterns According to S/C and R/L Bits

S/C	R/L	Operation
0	0	Shift cursor to the left, AC is decreased by 1
0	1	Shift cursor to the right, AC is increased by 1
1	0	Shift all the display to the left, cursor moves according to the display
1	1	Shift all the display to the right, cursor moves according to the display

Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	F	–	–

DL : Interface Data Length Control Bit
When DL = "High", it means 8-bit bus mode with MPU.
When DL = "Low", it means 4-bit bus mode with MPU. So to speak, DL is a signal to select 8-bit or 4-bit bus mode.
When 4-bit bus mode, it needs to transfer 4-bit data by two times.

N : Display Line Number Control Bit
When N = "Low", it means 1-line display mode.
When N = "High", 2-line display mode is set.

F : Display Font Type Control Bit
When F = "Low", it means 5 × 8 dots format display mode
When F = "High", 5 × 11 dots format display mode.

Set CGRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC. This instruction makes CGRAM data available from MPU.

Set DDRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC. This instruction makes DDRAM data available from MPU. When 1-line display mode (N = 0), DDRAM address is from "00H" to "4FH". In 2-line display mode (N = 1), DDRAM address in the 1st line is from "00H" to "27H", and DDRAM address in the 2nd line is from "40H" to "67H".

Read Busy Flag & Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether S6A0069 is in internal operation or not. If the resultant BF is High, it means the internal operation is in progress and you have to wait until BF to be Low, and then the next instruction can be performed. In this instruction you can read also the value of address counter.

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Write Data to RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM. The selection of RAM from DDRAM, CGRAM, is set by the previous address set instruction (DDRAM address set, CGRAM address set). RAM set instruction can also determine the AC direction to RAM. After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

Read Data from RAM

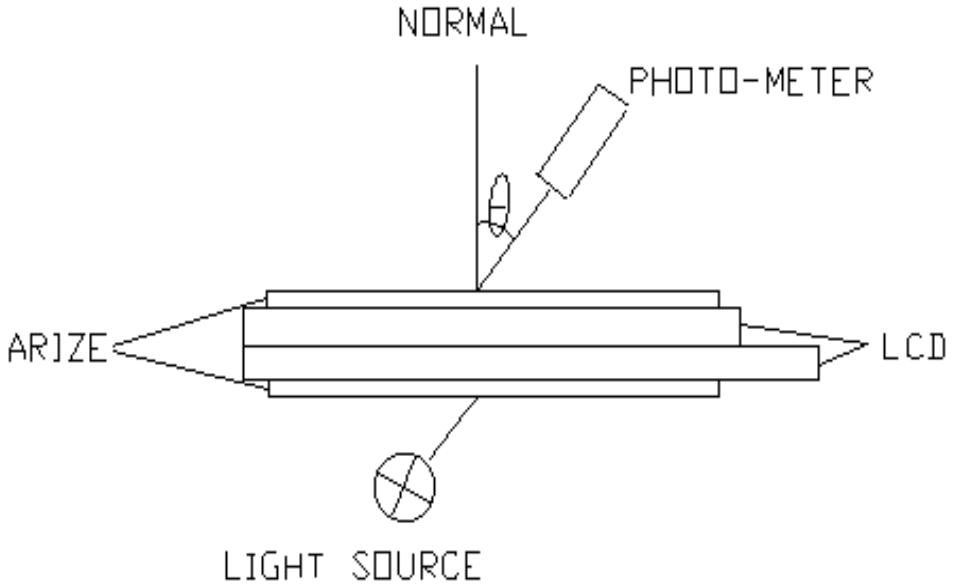
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM. The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, because the direction of AC is not determined. If you read RAM data several times without RAM address set instruction before read operation, you can get correct RAM data from the second, but the first data would be incorrect, because there is no time margin to transfer RAM data. In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction : it also transfers RAM data to output data register. After read operation address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM read operation, display shift may not be executed correctly.

NOTE

In case of RAM write operation, after this AC is increased/decreased by 1 like reading operation. In this time, AC indicates the next address position, but you can read only the previous data by read instruction.

11.0 PTICAL MEASUREMENT SYSTEM



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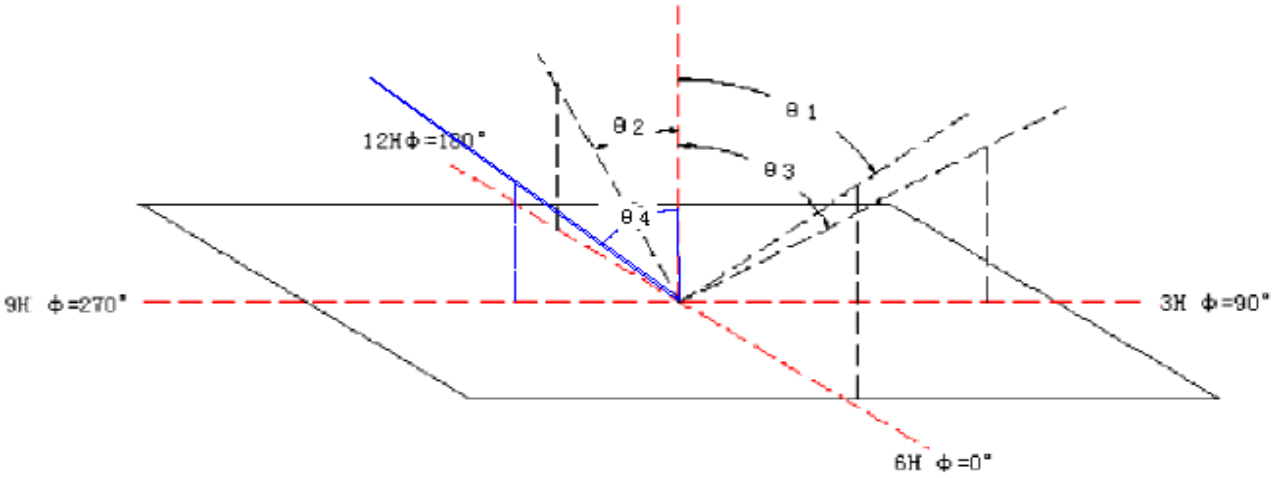
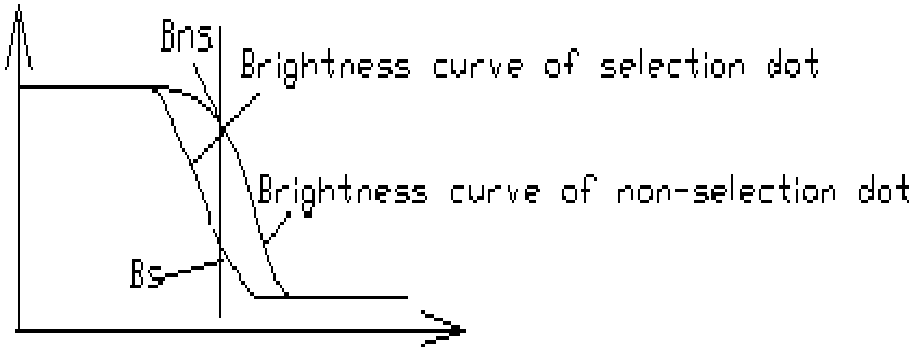
.DEFINITION OF θ AND Φ



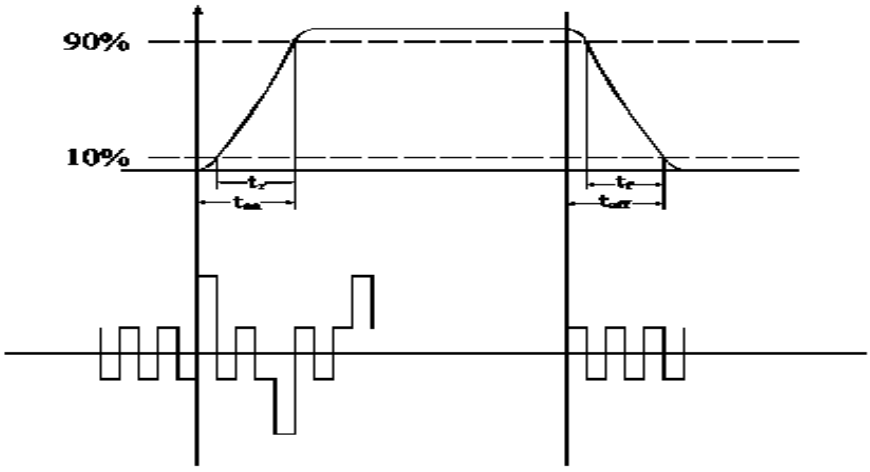
.DEFINITION OF CONTRAST RATIO Cr

DEFINITION:

$$Cr = \frac{\text{Brightness of non-selection dot (bns)}}{\text{Brightness of selection dot (bs)}}$$



.DEFINITION OF OPTICAL RESPONSE TIME



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